IT IS CLAIMED:

1. For a non-volatile memory comprising a plurality of storage elements formed upon a well structure, a method of erasing a selected one of said storage elements comprising:

concurrently charging the well structure and a control gate of said storage elements to an erase voltage; and

subsequently allowing the control gate of the selected storage element to discharge while maintaining the erase voltage on the well structure and the non-selected control gates.

2. The method of claim 1, wherein said maintaining comprises trapping charge on the well structure and the non-selected control gates while allowing the control gate of the selected storage element to discharge.

3. The method of claim 2, wherein said maintaining further comprises refreshing the charge level trapped on the well structure.

4. The method of claim 3, wherein said maintaining further comprises refreshing the charge level trapped on the non-selected control gates concurrently with refreshing the charge level trapped on the well structure.

5. The method of claim 2, wherein said maintaining further comprises refreshing the charge level trapped on the non-selected control gates.

6. The method of claim 1, wherein said plurality of storage elements are included in an array of such storage elements and wherein the control gates of the array's storage element are connected to word-lines whereby the voltage level of the control gates is set.

7 The method of claim 6, wherein the array is part of a first chip, further comprising:

generating the said erase voltage on a second chip; and

transferring the erase voltage to the first chip for use in said concurrently charging the well structure and a control gate of each of said storage elements.

8. For a non-volatile memory comprising a plurality of storage elements formed upon a well structure and capacitively coupled thereto, a method comprising:

selecting one or more but less than all of said storage elements for erase;

holding the well structure at an erase voltage;

concurrently with holding the well structure at the erase voltage, raising the voltage level on a control gate of the non-selected storage elements above that which results from the capacitive coupling to the well structure; and

concurrently with holding the well structure at the erase voltage, lowering the voltage level on a control gate of the selected storage elements to below the erase voltage.

9. The method of claim 8, wherein said raising the voltage level on a control gate of the non-selected storage elements above that which results from the capacitive coupling to the well structure comprises:

charging the control gate of each of the non-selected storage elements to the erase voltage concurrently with charging the well structure and subsequently maintaining the erase voltage on the non-selected control gates.

10. The method of claim 8, wherein said lowering the voltage level on the control gate of the selected storage elements comprises:

allowing the control gate of the selected storage elements to discharge

11. A non-volatile memory comprising:

a plurality of storage units formed upon a substrate;

a well structure in the substrate upon which the storage units are formed; and

control circuitry connectable to the substrate and a control gate of each of the plurality storage units whereby the voltage level of the well structure and said control gates may be concurrently set to an erase voltage, and further whereby the control gate of selected ones of the storage elements may be allowed to discharge the erase voltage while maintaining the erase voltage on the well structure and non-selected ones of the storage elements.

12. The non-volatile memory of claim 11, wherein the storage units are arranged into a plurality of rows, further comprising:

a plurality of word lines each connecting the storage elements of a respective row whereby said control circuitry is connectable to the control gate of each of the plurality storage units.

13. The non-volatile memory of claim 12, wherein the storage units form part of an array having a NAND architecture.

14. The non-volatile memory of claim 12, wherein the control circuit allows the selected control gates to discharge by connecting the respective word line to ground.

15. The non-volatile memory of claim 14, wherein the control circuit maintains the erase voltage on the non-selected storage elements by trapping charge on the on the respective word lines.

16. The non-volatile memory of claim 14, wherein the control circuit maintains the erase voltage on the well structure by refreshing the charge level trapped on the well structure.

17. The non-volatile memory of claim 16, wherein the control circuit maintains the erase voltage on the non-selected control gates by refreshing the charge level trapped on corresponding word lines concurrently with refreshing the charge level trapped on the well structure.

18. The non-volatile memory of claim 14, wherein the control circuit maintains the erase voltage on the non-selected control gates by refreshing the charge level trapped on corresponding word lines.

19. The non-volatile memory of claim 12, wherein the non-volatile memory is physically organized into a plurality of erase units each consisting of a

plurality of said word lines, and wherein said control circuitry selects the word lines of a given unit of erase for erase as a group.

20. The non-volatile memory of claim 11, wherein the storage units are multi-state storage units.

21. The non-volatile memory of claim 20, wherein the memory is a flash memory.

22. The non-volatile memory of claim 11, wherein the erase voltage is supplied to the control circuit from external to the memory.

23. A system, comprising:

a memory, comprising:

a plurality of non-volatile storage units formed upon a substrate and arranged into a plurality of rows and forming one or more columns;

a well structures in the substrate upon which the storage units are formed;

a plurality of word lines each connecting a respective control gate of each storage elements of a respective row; and

control circuitry connectable to the substrate and the world lines whereby the voltage level of the well structure and said control gates may be concurrently set to an erase voltage, and further whereby the control gate of selected ones of the storage elements may be allowed to discharge the erase voltage while maintaining the erase voltage on the well structure and non-selected ones of the storage elements;

a voltage source connectable to the memory wherein the erase voltage is generated; and

a controller connected to the memory for selecting memory cells for erase.

24. The system of claim 23, wherein the voltage source is on the same chip as the memory.

25. The system of claim 23, wherein the voltage source is on a different chip than the memory.

26. A non-volatile memory comprising:

a plurality of storage units formed upon a substrate;

a well structure in the substrate upon which the storage units are formed; and

means for maintaining, during an erase process of selected storage elements, the well structure and non-selected ones of the storage elements at an erase voltage while allowing the control gates of the selected storage elements to discharge.